Register No : _____

THE KAVERY ENGINEERING COLLEGE

(An Autonomous Institution)

M.E DEGREE END SEMESTER THEORY EXAMINATIONS, NOV /DEC 2024

Second Semester

Applied Electronics

AP4003- VLSI Design Techniques

Regulations - 2021

Duration : 3 Hrs *Maximum : 100 Marks*

*PART – A (ANSWER ALL QUESTIONS) (Marks 10*2=20)*

Q.No	*Questions*	*BLT*	*CO*	*Marks*
1.	What is the threshold voltage V_{th} of an MOS transistor?	RE	1	2
2.	List the steps in the VLSI design flow.	RE	1	2
3.	State the importance of interconnect.	RE	2	2
4.	Compare procedural assignments and continuous assignments in Verilog.	UN	2	2
5.	Define clock skew.	RE	3	2
6.	How does metastability occur in static latches?	UN	3	2
7.	Justify the need for testing in CMOS.	UN	4	2
8.	List some advantage of boundary scan.	RE	4	2
9.	Write a Verilog code for 2 input AND gate.	UN	5	2
10.	List three examples of gate primitives in Verilog HDL.	RE	5	2

*PART – B (ANSWER ALL QUESTIONS) (Marks 5*13 = 65)*

Q.No			*Questions*	*BLT*	*CO*	*Marks*
11.	a		Explain in detail the I-V characteristics of MOS transistors.	UN	1	13
			Or			
	b	i	Outline the important rules for creating stick diagrams.	UN	1	4
		ii	Classify and explain the different types of layout design rules in CMOS technology.	UN	1	9
12.	a	i	Analyze how the concept of logical effort can be applied to optimize circuit performance.	AN	2	6
		ii	Analyze the two main components of power dissipation and compare its performance for static CMOS circuits.	AN	2	7
			Or			
	b		Classify and explain the different types of modeling techniques used for the design of combinational and sequential circuits in HDL.	AN	2	13
13.	a	i	Discuss the variety of circuit pitfalls that can cause chips to fail.	UN	3	6
		ii	Illustrates how time borrowing can effectively optimize circuit design in pipelined architectures.	UN	3	7
			Or			

	b	i	How do the designs of transparent latches improve their performance in terms of output swing, noise immunity, and stability?	UN	3	6
		ii	Discuss the importance of synchronizers in enabling reliable communication between asynchronous clock domains.	UN	3	7
14.	a	i	Discuss the setup procedures of a test program for CMOS circuit testing.	UN	4	6
		ii	Explain the various techniques employed in silicon debugging to directly access and diagnose issues in integrated circuits.	UN	4	7
			Or			
	b		Explain the main approaches commonly used to design for testability.	UN	4	13
15.	a	i	Explain the concept of procedural assignments in Verilog HDL.	UN	5	6
		ii	Explain how a combinational circuit, specifically a 4-input multiplexer, can be designed using dataflow modeling in Verilog.	UN	5	7
			Or			
	b	i	Discuss the HDL behavioral modeling approaches in Verilog.	UN	5	7
		ii	Discuss the use of test benches in the verification of digital designs in Verilog.	UN	5	6

*PART – C (Marks 1*15 = 15)*

Q.No			*Questions*	*BLT*	*CO*	*Marks*
16.	a		Design a 4 bit ripple carry adder using dataflow model and structural modelling in Verilog HDL.	AN	2	15
			Or			
	b		Design of 4:1 multiplexer using two 2:1 multiplexer by structural modelling in Verilog HDL.	AN	5	15